SEMICONDUCTOR DEVICE TEST PATTERNS AND RELATED METHODS FOR PRECISELY MEASURING LEAKAGE CURRENTS IN SEMICONDUCTOR CELL TRANSISTORS

Abstract of the Disclosure

Semiconductor device test patterns are provided that include a word line on a semiconductor substrate and an active region having a first impurity doped region and a second impurity doped region in at the semiconductor substrate. A first self-aligned contact pad is electrically connected to the first impurity doped region, and a first direct contact is electrically connected to the first self-aligned contact pad. A first bit line is electrically connected to the first direct contact, and a first probing pad is electrically connected to the first bit line. The test pattern further includes a second self-aligned contact pad that is electrically connected to the second impurity doped region, and a second direct contact electrically connected to the second self-aligned contact pad. A second conductive line is electrically connected to the second direct contact, and a second probing pad is electrically connected to the second conductive line. These test patterns may be used to measure leakage current in a cell transistor of the semiconductor device.